* * * R*E*M*A*R*K*S * * *

Applicant herewith submits this Amendment in a bona fide attempt to advance the prosecution of this case and to answer each and every ground of rejection as set forth by the Examiner. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments to the specification and claims, and the remarks set forth below.

1. Misspelling of Inventor Name

Applicant would like to point out that the inventor's name listed in paper 7 (Form PTO-90 dated 05/21/2003) under "FIRST NAMED INVENTOR" as Tohmas Eugene Washura should be corrected to read "Thomas Eugene Waschura"

2. Amendment to Specification and Claims

In this response, Applicant has amended the above-noted portions of the specification and enumerated claims to correct minor typographical and grammatical error present therein. The Applicant submits that no new matter has been added by such amendments.

3. Rejection of Claims 1-7

The Examiner has rejected Claims 1-7 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

Claim 1 is directed to an apparatus for measuring characteristics of a bit stream of binary pulses and includes the following limitations:

"...control means for defining a window comparator..." and

> "...logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics..."

that are not disclosed in Deisch. Consequently, Deisch does not anticipate the invention as defined in Claim 1. In rejecting Claim 1, the Examiner states, in relevant part, that:

> "...Deisch discloses an apparatus for measuring characteristics of a bit stream of binary pulses comprising control means for defining a window comparator (abstract, fig. 8)..."

However, a thorough review of the abstract does not disclose or otherwise uncover the "...control means for defining a window comparator..." language as asserted by the Examiner. Consequently, the Examiner has not provided Applicant with a location within Deisch where such limitation is disclosed. Accordingly, the Applicant submits that the Examiner's interpretation and statements regarding Deisch are improper and should be withdrawn, and at least this limitation of Claim 1 is not anticipated by Deisch.

Further, the Applicant would like to point out that the claimed invention and the circuit disclosed in Deisch appear to be directed to dissimilar technologies; thereby, making Deisch an improper reference under 35 U.S.C. §102. More specifically, the invention as claimed, for example, in Claim 1 is directed to "An apparatus for measuring characteristics of a bit stream..." In contrast, as specifically recited, for example, at col. 2, lines 41-42; col. 4, lines 52-53 and col. 5, lines 48-50, Deisch is directed to a pulse shaping and filtering circuit. Nowhere, within Deisch is there a discussion of any characteristic measurement or anything equivalent thereto. Thus, the Applicant submits that Deisch is directed to subject matter different from that defined in the claims. Accordingly, Deisch is an improper reference and should be withdrawn.

Notwithstanding the inappropriateness of Deisch as a reference, Claim 1 further includes I a limitation directed to:

> "...logic means for accumulating event counts of the bit stream pulses falling within points inside the window comparator during durations of the binary pulse bit stream and drawing eye diagrams therefrom defining the bit stream characteristics..."

which is also not disclosed in Deisch. Consequently, Deisch does not anticipate this limitation of Claim 1. As stated above, Deisch is silent on its circuit including or even using a "window comparator"; therefore, that portion of the above recited limitation is not disclosed in Deisch. Also, Deisch is silent on any means of "...drawing eye diagrams therefrom defining the bit stream characteristics..." as no means of displaying any information is present in Deisch. The Examiner is reminded that Deisch is self-admittedly directed to a "...pulse shaping and filtering circuit" that does not have the capability to display any information. The Examiner appears to interpret the output representations of Fig. 5 and 7 as being the display means. However, a more accurate characterization of such figures is that they are "...component waveforms...generated by the circuit..." (See, for example, col. 3, lines 23-24) that are used to illustrate a possible output of the signal; not the actual signal output. As no display or other suitable output mechanism is disclosed in Deisch, no "...logic means for drawing eye diagrams..." is disclosed in Deisch.

Moreover, as no accumulation of information is provided by the pulse shaping and filtering circuit of Deisch, no "...logic means for accumulating event counts of the bit stream pulses..." is disclosed in Deisch. Consequently, at least this limitation of Claim 1 is not disclosed in Deisch.

Thus, as Deisch is directed to a different technological area of the present invention and the aforementioned limitations are not disclosed in Deisch, the Applicant submits that Deisch does not anticipate the invention as defined in Claim 1. Accordingly, reconsideration of the rejection of Claim 1 is respectfully respected.

Claims 2-6 directly or indirectly depend upon and include the limitations of Claim1 and are allowable at least for the reasons set forth above with respect to Claim 1. Moreover, these claims include and define additional subject matter that is not disclosed in Deisch. More specifically, Claim 2 includes the limitation of:

> "...programmable means for establishing an array of columns and rows defining the points for accumulating counts of pulse voltage levels at time offsets during the duration times and for creating a voltage threshold window that moves between a minimum and maximum voltage with changes or rows of the array..."

and Claim 4 includes the limitation of:

> "...first counter mans for accumulating counts of the detected binary pulse voltage levels at the time offsets during each duration part of the binary pulse bit stream in a column and row point of the array..."

that are clearly not disclosed in Deisch. As discussed above, Deisch is silent on any mechanism for providing an eye diagram. Thus, Deisch is silent on any mechanism that is capable of establishing or providing "...an array of columns and rows defining the points for accumulating counts..." as defined, for example, in Claim 2. Moreover, as Deisch does not perform any accumulation functions, Deisch does not disclose "...first counter means for accumulating counts of the detected binary pulse voltage levels..." as defined, for example, in Claim 4. Consequently, Deisch does not anticipate the invention as defined in any of Claims 2-6. Accordingly, reconsideration of the rejection of Claims 1-6 is respectfully requested.

4. Rejection of Claim 7

The Examiner has rejected Claim 7 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

The inappropriateness of Deisch as a reference as discussed in greater detail above in Section 3 is equally applicable to Claim 7 and is incorporated in its entirety herein. Notwithstanding the inappropriateness of Deisch as a reference, it does not anticipate the invention as defined in Claim 7 as provided below.

Claim 7, like Claim 1 above, includes a limitation directed to:

> "...control means for defining a window comparator of an array of columns and rows defining points for accumulating voltage counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream..."

As such, Claim 7 is allowable at least for the reasons set forth above with respect to Claim 1. Accordingly, reconsideration of the rejection of Claim 7 is respectfully requested.

Further, Claim 7 also includes a limitation directed to:

> "...apparatus for creating a voltage threshold window that moves between minimum and a maximum voltage levels with each row of the array and for accumulating counts of voltage levels of the binary pulses occurring at the time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array and displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses..."

that is also not disclosed in Deisch. As stated in Section 3 above, Deisch is directed to a "...pulse shaping and filtering circuit..." (See, for example, col. 2, lines 41-42; col. 4, lines 52-53 and col. 5, lines 48-50). Nowhere within the reference is there any discussion of any apparatus or component that is capable of "...creating a voltage threshold window that moves between minimum and a maximum voltage levels with each row...and column point of the array..." and "...displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses..." as Deisch does not accumulate any

data nor display any data, accumulated or not- as Deisch does not disclose the use or requirement of a display. The Applicant respectfully points out to the Examiner that Deisch is directed to a stand alone shaping and filtering circuit; it is not directed to a circuit or apparatus using or requiring a display. As such, Deisch does not anticipate the invention as defined in Claim 7. Accordingly, reconsideration of the rejection of Claim 7 is respectfully requested.

5. Rejection of Claim 8

The Examiner has rejected Claim 8 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

The inappropriateness of Deisch as a reference as discussed in greater detail above in Section 3 is equally applicable to Claim 8 and is incorporated in its entirety herein. Notwithstanding the inappropriateness of Deisch as a reference, it does not anticipate the invention as defined in Claim 8 as provided below.

Claim 8, like Claim 1 above, includes a limitation directed to "...first control means for defining a window comparator..." As such, Claim 8 is submitted to be allowable at least for the reason set forth above with respect to Claim 1.

Further, Claim 8 includes additional limitations that are not disclosed or otherwise taught or suggested in Deisch. More specifically, Claim 8 includes limitations directed to:

> "...second control means for creating a voltage threshold window that moves between a minimum and maximum voltage threshold with each row of the array..." and
>
> "...logic means for detecting voltage levels of the binary pulses occurring at time offsets of the bit stream when the pulse voltage levels are within the voltage threshold at each row and column point of the array..."

that are not disclosed or otherwise taught in Deisch. As discussed in greater detail above, Deisch is directed to a pulse shaping and filter circuit that is not capable of displaying resulting values (due to no display or other suitable device being provided thereby). Additionally, it should be pointed out that the circuit disclosed in Deisch is a stand alone circuit that completes its functions without the requirement or need for array row and column points. As Deisch is silent on the need for generating or otherwise using array row and column points and the detection thereof, the Applicant submits that Deisch does not anticipate the aforementioned limitations of Claim 8.

Moreover, Claim 8, like Claim 7 above, includes limitations directed to:

> "...first counter means for detecting accumulating counts of the detected binary pulse voltage levels at time offsets during each defined duration time of the binary pulse bit stream in a column and row point of the array..." and
>
> "...second counter means for determining duration of periods of the binary bit stream in which to accumulate the detected binary pulse voltage levels at each point of the array..."

that are not disclosed or otherwise discussed in Deisch. As discussed in greater detail in Section 4, Deisch does not perform, nor is there a discussion or a requirement or need to perform any accumulation operations on the incoming data stream. As accumulation is neither required nor disclosed in Deisch, the Applicant submits that the aforementioned limitations of Claim 8 are not anticipated by Deisch.

Finally, Claim 8 includes a limitation directed to:

> "...monitor apparatus for displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses..."

Such limitation is neither disclosed nor suggested in Deisch. As discussed in greater detail above, Deisch does not disclose a mechanism for displaying the accumulated data. The Examiner misstates or misinterprets Figures 5 and 7 as being equivalent to a

display or suitable monitor; however, as clearly articulated in Deisch, for example at col. 3, lines 23-24, such figures are representations of "...component waveforms...generated by the circuit..." that are used to illustrate a possible output of the signal; not the actual signal output. As such, as Deisch does not disclose a monitor or other suitable apparatus for displaying the accumulated information, the Applicant submits that the aforementioned limitation is not disclosed in Deisch.

Consequently, as none of the aforementioned limitations are disclosed in Deisch, the Applicant submits that Deisch does not anticipate the invention as defined in Claim 8. Accordingly, reconsideration of the rejection of Claim 8 is respectfully requested.

6. Rejection of Claims 9-14

The Examiner has rejected Claim 9 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

The inappropriateness of Deisch as a reference as discussed in greater detail above in Section 3 is equally applicable to Claim 9 and is incorporated in its entirety herein. Notwithstanding the inappropriateness of Deisch as a reference, it does not anticipate the invention as defined in Claim 9 as provided below.

Claim 9 is a method claim that recites operating steps that may be performed, for example, on the apparatus defined in Claim 1. Claim 9 includes the step of "...defining a window comparator..." which, as discussed in greater detail in Section 3, is not disclosed or otherwise taught in Deisch. As such, the Applicant submits that at least this limitation of Claim 9 is not anticipated by Deisch.

Further, Claim 9 includes the step of:

"...accumulating event counts of the bit stream pulses at time offsets during defined duration times of the binary pulse bit stream at points inside

> the window comparator and drawing an eye diagram therefrom defining the bit stream pulse characteristics..."

which is not disclosed or otherwise taught in Deisch. As discussed in greater detail in Sections 4 and 5, Deisch does not disclose the use, requirement, necessity or desirability of either accumulating bit pulse information or displaying the same. Deisch is directed to a pulse shaping and filtering circuit that provides an output signal having smooth (e.g. sinusoidal) transitions between transition points. Nowhere within Deisch is there a reference or discussion of an accumulation mechanism. Nor has the Examiner provided a proper location within Deisch to where such function or discussion is presented. As the Examiner has not provided a proper location within Deisch as to where the aforementioned limitations can be found, and the Applicants have not found a location within Deisch where such discussion can be found, the Applicant submits that Deisch does not anticipate at leas the aforementioned limitations of Claim 9. Accordingly, reconsideration of the rejection of Claim 9 is respectfully requested.

Claims 10-14 directly or indirectly depend upon and include the limitations of Claim 9 and are allowable at least for the reasons set forth above with respect to Claim 9. Moreover, these claims define subject matter that is also submitted to be allowable over the art of record. More specifically, Claim 10 includes the limitation directed to:

> "...establishing an array of columns and rows defining the points for accumulating the event counts at time offsets during the defined duration times..."

which is clearly not disclosed in Deisch. As stated in more detail above, Deisch does not disclose the use or need for displaying any information. Deisch is directed to and discloses a stand alone circuit that shapes and filters incoming data. It does not display nor provide arrays of columns and rows for defining accumulation points as recited in Claim 10.

Moreover, Claims 13 and 14 include limitations directed to:

"...accumulating counts of detected binary pulse voltage levels..." and

"...displaying the array column and row points of accumulated event counts as an eye diagram..."

that are clearly not disclosed in Deisch. As discussed in greater detail above, the functions of accumulating and displaying the accumulated information are not disclosed in Deisch as Deisch does not disclose the use or presence or an accumulation mechanism. A delay circuit is present in the circuit, operative to delay by a predetermined amount of time the input thereto; however, this delay circuit is not the same as or analogous to an accumulator. Therefore, the step of accumulating counts of detected binary pulse voltage levels is not disclosed in Deisch. As Deisch does not disclose the use of a display, the limitation of "...displaying the array column and row points of accumulated event counts..." cannot and is not present in Deisch. Therefore, the invention as defined in the aforementioned claims is not anticipated by Deisch. Accordingly, reconsideration of the rejection of Claims 9-14 is respectfully requested.

7. Rejection of Claim 15

The Examiner has rejected Claim 15 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

The inappropriateness of Deisch as a reference as discussed in greater detail above in Section 3 is equally applicable to Claim 15 and is incorporated in its entirety herein. Notwithstanding the inappropriateness of Deisch as a reference, it does not anticipate the invention as defined in Claim 15 as provided below.

Claim 15 is a method claim which defines the operations performed, for example, by the apparatus defined in Claims 1 and 7. Claim 15, like Claim 9 above, includes limitations directed to:

> "...defining a window comparator of an array of columns and rows defining points for accumulating event counts of the binary pulse bit stream at time offsets during defined durations of the binary pulse bit stream..."and
>
> "...accumulating counts of voltage levels of the binary pulses occurring at time offsets of the bit stream during a duration time when the pulse voltage levels are within the voltage threshold window at each row and column point of the array..."

As such, Claim 15 is submitted to be allowable at least for the reasons set forth above with respect to Claim 9.

Further, Claim 15 also includes a limitation directed to:

> "...displaying the array column and row points of the accumulated event counts as an eye diagram defining characteristics of the bit stream of binary pulses..."

which as discussed in greater detail in Section 6, above, is not disclosed in Deisch as Deisch does not disclose the presence or use of a display or any suitable device. As such, this limitation is not anticipated by Deisch.

Moreover, Claim 15 includes the following limitation:

> "...creating a voltage threshold window that moves between a minimum voltage and a maximum voltage at each row of the array..."

which is also not disclosed or other taught in Deisch. At best, Deisch provides a representation of an output waveform when a pulse is applied to the circuit of Fig. 6. The circuit illustrated, for example, in Fig. 8 appears to only generate a shaped output wave in response to a pulse input. Contrary to the Examiner's assertions, Deisch does not appear to create a voltage threshold window that moves between a minimum and maximum voltage at each row of the array. As such, the aforementioned limitation of Claim 15 is also not disclosed in Deisch.

Consequently, as none of the aforementioned limitations of Claim 15 is disclosed in Deisch, the Applicant submits that Deisch does not anticipate the invention as

defined in Claim 15. Accordingly, reconsideration of the rejection of Claim 15 is respectfully requested.

8. Rejection of Claim 16

The Examiner has rejected Claim 16 under 35 U.S.C. §102(b) as being anticipated by Deisch (U.S. Patent No. 6,072,340). The Applicant traverses such rejection for the reasons set forth in greater detail below.

The inappropriateness of Deisch as a reference as discussed in greater detail above in Section 3 is equally applicable to Claim 16 and is incorporated in its entirety herein. Notwithstanding the inappropriateness of Deisch as a reference, it does not anticipate the invention as defined in Claim 16 as provided below.

Claim 16 is a method claim which defines the operations performed, for example, by the apparatus defined in Claims 1 and 7. Claim 16, like Claim 15 above, includes limitations directed to:

> "...defining a window comparator of an array of columns and rows defining points for accumulating event counts at time offsets during defined duration times of the binary pulse bit stream...";
>
> "...accumulating counts of the detected binary pulse voltage levels at the offsets in a column and row point of the array..." and
>
> "...displaying the array column and row points of the accumulated time and voltage counts as an eye diagram defining characteristics of the bit stream of binary pulses..."

As such, Claim 16 is allowable at least for the reasons set forth above with respect to Claim 15. Accordingly, the Applicants submit that the aforementioned limitations of Claim 16 are not disclosed in Deisch.

Further, Claim 16 includes a limitation directed to:

> "...creating a voltage threshold window that moves between defined voltage levels at each row of the array..."

which is also not disclosed or otherwise taught in Deisch. As discussed above, and further presented in Section 7, as Deisch does not disclose defining a window comparator or an array of columns and rows, Deisch cannot create a voltage threshold window that moves between defined voltage levels at each row of the array as there are no rows to traverse. Additionally, as understood, Deisch provides a representation of an output waveform when a pulse is applied to the circuit of Fig. 6. The circuit illustrated, for example, in Fig. 8 appears to only generate a shaped output wave in response to a pulse input. Contrary to the Examiner's assertions, Deisch does not appear to create a voltage threshold window that moves between "defined voltage levels at each row of the array." As such, the aforementioned limitation of Claim 16 is also not disclosed in Deisch.

Finally, Deisch does not disclose the following limitation of Claim 16:

> "...detecting voltage levels of the binary pulses occurring at the time of the bit stream when the pulse voltage levels are within the voltage threshold window at each row and column point of the array..."

as a threshold window, having corresponding rows and columns is not disclosed as being provided by Deisch. For example, as explicitly stated at col. 4, lines 51-64 and col. 5, line 48-col. 6, line 2, Deisch disclosed a shaping and filtering circuit. There is no discussion within Deisch of providing a window or anything analogous thereto having or being separated into row and columns. As such functionality is not disclosed in Deisch, the aforementioned detecting operation cannot and is not performed by Deisch. Consequently, the aforementioned limitation of Claim 16 is not disclosed in Deisch.

Thus, as none of the aforementioned limitations of Claim 16 is disclosed in Deisch, the Applicants submit that Deisch does not anticipate the invention as defined

in Claim 16. Accordingly, reconsideration of the rejection of Claim 16 is respectfully requested.

CONCLUSION

In summary, Applicant has reviewed and amended the specification and claims 15 and 16 and believes they are in condition for allowance. In view of the arguments herein set forth, Applicant respectfully submits that claims 1 through 16 distinguish over the art cited by the Examiner and are allowable. Applicant, having answered each and every ground of rejection set forth by the Examiner, now submits that the case is in proper condition for allowance and such action is earnestly solicited.

If any questions should arise with respect to the above remarks, or if it would in any way expedite the prosecution of this case, Applicant's attorney would appreciate a telephone call at (408) 965-4001.

Respectfully submitted,

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